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WO 1997/045870 A2 US 6119175 A
US 5594874 A US 4991085 A
US 4717912 A

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(54) Abstract Title
Multi-use pins on ASIC

(57) An ASIC (Application Specific Integrated Circuit) (40)comprises a plurality of internal communication buses (46, 48, 50), a plurality of pins for connecting external devices to the ASIC (40), and means for selecting one of the buses to which each pin is connected.

The means for selecting is particularly a multiplexer (52) and the buses may be an address bus (46), a data bus (48) or a control bus (50). It is also preferable that at least some of the pins are bidirectional.

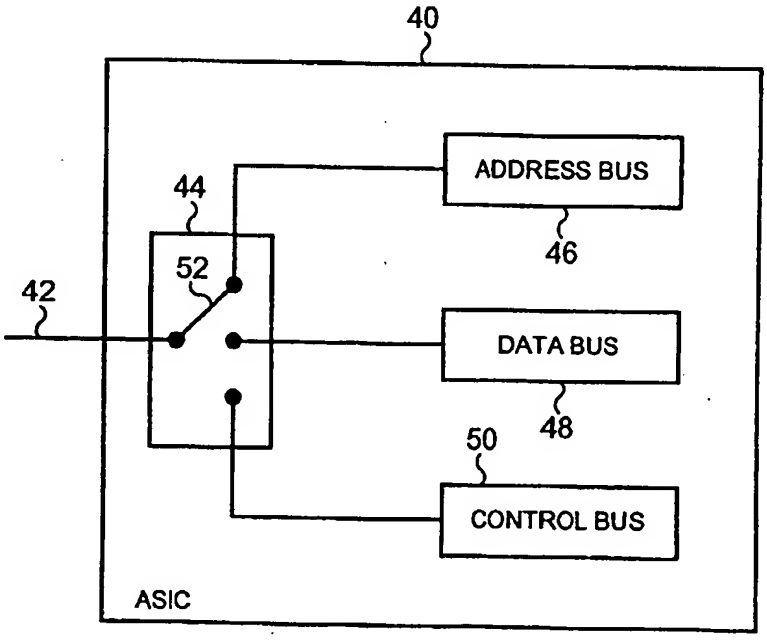

FIG. 5

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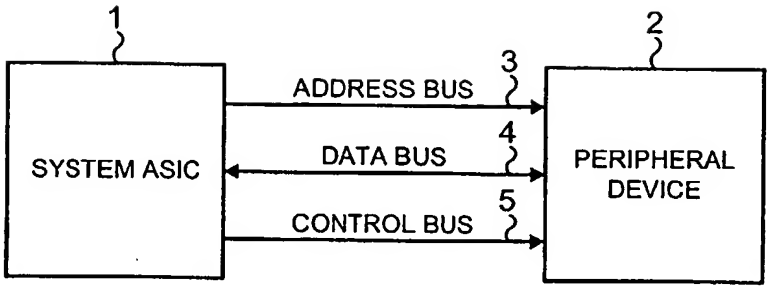
1
2
3
ADDRESS BUS
4
DATA BUS
5
CONTROL BUS
SYSTEM ASIC
PERIPHERAL DEVICE

FIG. 1

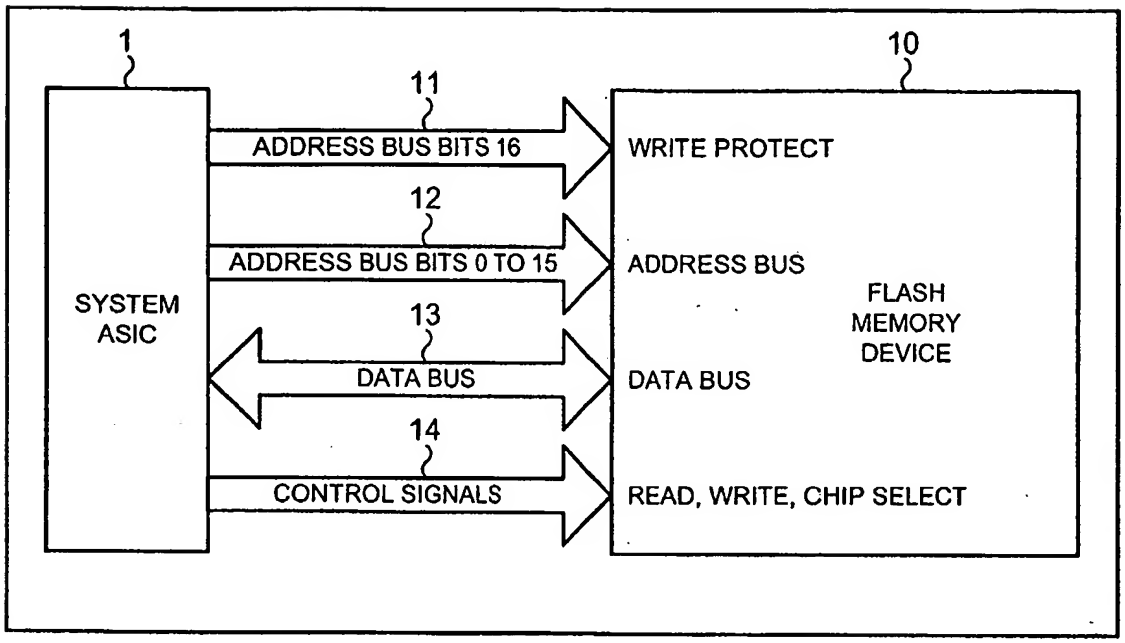
1
10
11
ADDRESS BUS BITS 16
WRITE PROTECT
12
ADDRESS BUS BITS 0 TO 15
ADDRESS BUS
SYSTEM ASIC
FLASH MEMORY DEVICE
13
DATA BUS
DATA BUS
14
CONTROL SIGNALS
READ, WRITE, CHIP SELECT

FIG. 2

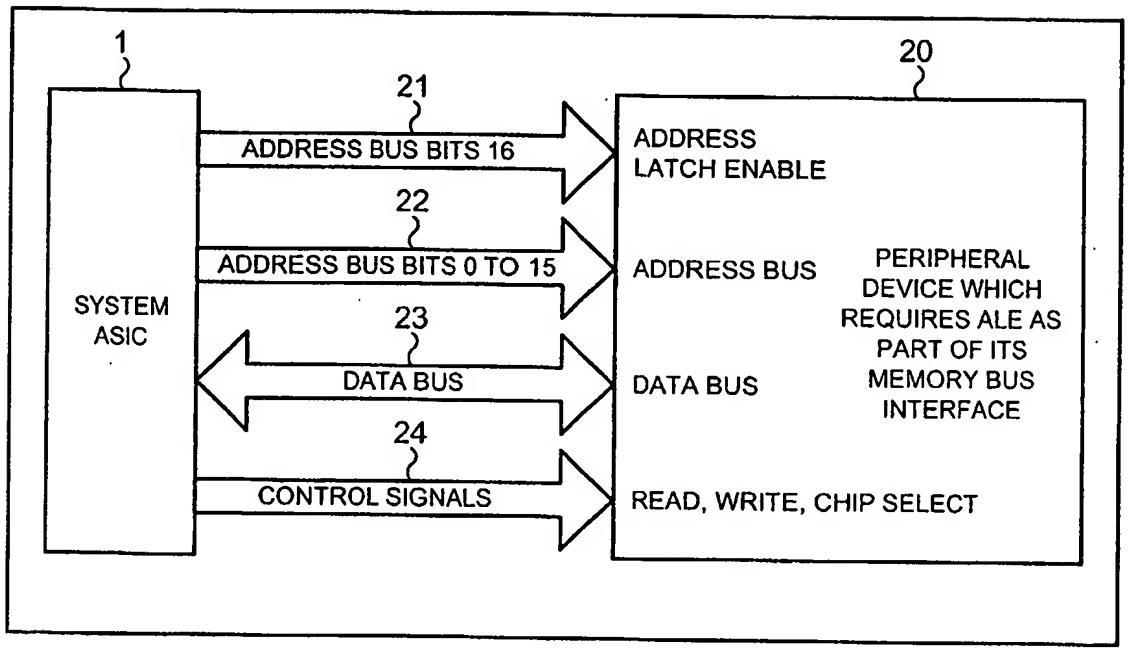
1
20
21
ADDRESS BUS BITS 16
ADDRESS
LATCH ENABLE
22
ADDRESS BUS BITS 0 TO 15
ADDRESS BUS
PERIPHERAL
DEVICE WHICH
REQUIRES ALE AS
PART OF ITS
MEMORY BUS
INTERFACE
SYSTEM
ASIC
23
DATA BUS
DATA BUS
24
CONTROL SIGNALS
READ, WRITE, CHIP SELECT

FIG. 3

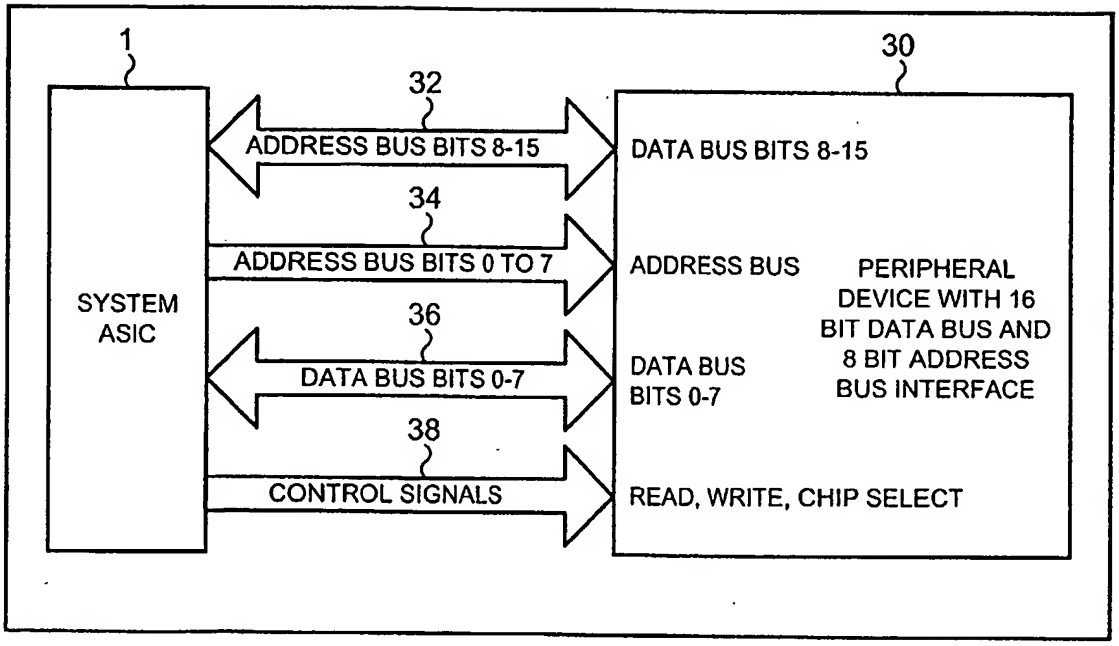
1
30
32
ADDRESS BUS BITS 8-15
DATA BUS BITS 8-15
34
ADDRESS BUS BITS 0 TO 7
ADDRESS BUS
PERIPHERAL DEVICE WITH 16 BIT DATA BUS AND 8 BIT ADDRESS BUS INTERFACE
SYSTEM ASIC
36
DATA BUS BITS 0-7
DATA BUS BITS 0-7
38
CONTROL SIGNALS
READ, WRITE, CHIP SELECT

FIG. 4

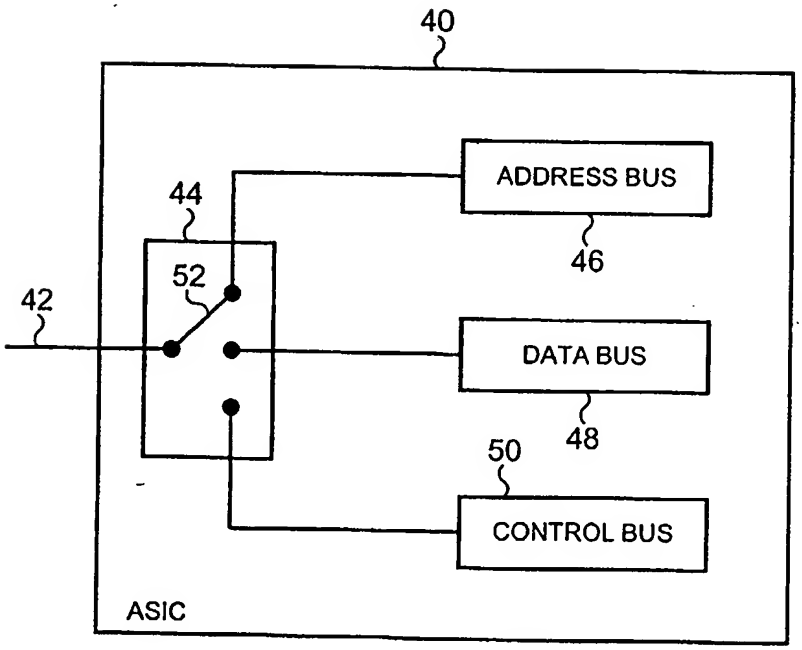

FIG. 5

Use of pins on an ASIC

The present invention relates to the use of pins on an ASIC.

Modern systems often incorporate one or more ASIC devices which include a processor core. Typically the system ASIC uses an address bus and data bus to communicate with other devices in the system such as memory and peripherals. Generally a particular pin may only transfer one type of signal; either address signals, data signals or control signals. Therefore the pins may be described as address pins, data pins or control pins.

Different devices require different numbers of address pins. When the core addresses a particular peripheral device it may be the case that the peripheral does not utilise all of the available address pins which are supplied by the system ASIC. In this situation the unused address pins are redundant.

One design constraint on ASIC devices as commonly used in modern system design is the number of pins available on a package. This is of particular importance when a 32-bit microprocessor is included within the device as this uses a large number of pins simply for the memory interface.

Embodiments of the present invention facilitate the use of any address pin, which is not required to transfer address signals when interfacing a particular device, to be used for alternate purposes such as supplying extra control signals to the peripheral device. In this way the number of pins required is reduced. Therefore a more efficient usage of pins is obtained when communicating with external devices. Increasing the number of communication channels

between the processor and the device will reduce the communication time to any device, minimise the size of the ASIC package required and reduce the number of tracks required to be routed to the package on the PCB.

According to the present invention there is provided an ASIC comprising a plurality of internal communication buses, a plurality of pins for connecting external devices to the ASIC, and means for selecting the internal communication bus to which each pin is connected.

According to the present invention there is further provided a method for enabling an ASIC to communicate with an external device, the ASIC comprising a plurality of communication buses, a plurality of pins and means for selecting the internal communication bus to which each pin is connected, the method comprising the steps of: connecting at least some of the pins to the external device and controlling the selecting means to connect a desired internal communication bus to each of the pins connected to the external device.

Preferred embodiments of the present invention will now be described with reference to the accompanying drawings in which;

Figure 1 shows a first embodiment of the present invention in use for communication between a system ASIC and peripheral device;

Figure 2 shows a second embodiment of the present invention in use for communication between a system ASIC and a flash memory device;

Figure 3 shows a third embodiment of the present invention in use for communication between a system ASIC and a

peripheral device which requires address latch enable as part of its memory bus interface;

Figure 4 shows a fourth embodiment of the present invention in use for communication between a system ASIC and a peripheral device with a 16 bit data bus and an 8 bit address bus interface.

Figure 5 shows a multiplexer for determining which signal is supplied by a particular pin.

Figure 1 shows a system ASIC 1 containing a processor core which is attached to a peripheral device 2 with bus width allocated to address bus 3, data bus 4 and control bus 5. The address bus 3 and control bus 5 only permit unidirectional signals from the system ASIC 1 to the peripheral device 2 but the data bus 4 permits bidirectional signals.

Figure 2 shows the system ASIC 1 of Figure 1 containing a processor core attached to a FLASH memory device 10 which does not require the complete address bus width. The system ASIC 1 provides 32 address bits. The number of address bits is not limited to 32 but can also be any higher or lower number. In the embodiment of Figure 2, only address bus bits 0-15 12 are required to address the FLASH memory device 10. Address bus bits 16-31 11 are redundant for the purposes of addressing the Flash Memory Device 10 and can be used to control the functions of the device 10. In this example the address bit 16 11 is used to control a Write Protect function which prevents erroneous writes to the device. Bidirectional data signals are sent between ASIC and device by data bus 13 and control signals sent at 14.

In the embodiment of Figure 2 the level of the write protect signal (Address bit 16) 11 during a FLASH access

cycle is determined by the address which is supplied to access the device 10. Therefore no additional bus is required within the ASIC to control the Write protect function. In Figure 2 if the device 10 has an address in the range 00000h to 0FFFFh then the address bus bits 16-31 11 are not required to address the device. Therefore address bus bit 16 11 is low thereby inhibiting writes to the flash.

In the embodiment of Figure 2 if the address of the device is in the range 10000h to 1FFFFh address bus bit 16 is high, thereby enabling writes to the flash.

The advantage of this method is that when the number of address bits required is smaller than the total number of address bits available, control of the write protect pin is achieved without having to use an extra pin on the ASIC 1.

In the preferred embodiment shown in Figure 3 the system ASIC 1 of Figure 1 is connected to a peripheral device 20 which requires an address latch enable (ALE) as part of its memory bus interface. In this embodiment only address bus bits 0-15 22 are required to address the device leaving address bits 16-31 21 available for supplying alternative signals. In the example of Figure 3 address bus bit 16 21 is used as a control signal with specific timings rather than as static address signals which are always at a fixed level during the bus access cycle as in Figure 2. Bidirectional data signals are transferred by data bus 23 and further control signals are sent from the system ASIC 1 to the device 20 at 24.

In the preferred embodiment shown in Figure 4 extra address pins are used to extend the width of the data bus between the system ASIC 1 and the peripheral device 30. In this embodiment the system ASIC 1 has an 8-bit data bus

36 and a 16-bit address bus 32 and 34. The system ASIC is communicating with a peripheral device 30 with a 16 bit wide data bus and an 8 bit address bus interface. In this case only 8 address bits of the system ASIC 1 are required to address the device 30. Address bus bits 8-15 32 are available to supply the additional 8 bits of data. In this example the address bus signals 32 from the system ASIC 1 have to be bidirectional in order to facilitate data input or output. In their normal function as address pins they are only required to be outputs. Therefore, in order to obtain full benefit in reducing pin numbers, it is preferable for at least some of the address pins on the ASIC to be bidirectional so that they can transmit or receive signals. The bidirectional address pins will usually be the most significant bits of the address bus, but all of the address pins could be bidirectional.

If the data bus width of the processor core is greater than that of the peripheral being accessed, the unused data lines can be used to control other signals in a similar fashion to the address lines described above. However, as the data lines are bi-directional this can only be used when writing to the device since when reading from it the unused data lines would be in input mode and therefore not drive any signals to the controlled device. For this reason, data lines can only be used for this purpose in write only devices.

Figure 5 shows the mechanism by which an individual pin 42 may be used to supply address, data or control signals to a peripheral device. The pin 42 is connected to either the address bus 46, data bus 48 or control bus 50 by means of a multiplexer 44. The multiplexer 44 provides a connection between the pin 42 and one of these buses by means of a switch 52.

A pin which is nominally allocated to supplying address signals will preferentially be connected to the address bus through the multiplexer. However, when communicating with a device which does not require the pin to carry address signals, the multiplexer can provide a connection from the pin to either the data bus or the control bus via the multiplexer.

Any or all of the pins from the ASIC can be connected to individual multiplexers to facilitate connection to either the address bus, data bus or control bus by the method described above and illustrated in Figure 5.

It will be clear to those skilled in the art that many variations to the embodiments described are possible without departing from the scope of the invention which is limited solely by the claims attached.

Claims

1. An ASIC comprising a plurality of internal communication buses, a plurality of pins for connecting external devices to the ASIC, and means for selecting the internal communication bus to which each pin is connected.

2. An ASIC according to claim 1 wherein the means for selecting the internal communication bus to which each pin is connected is a multiplexer.

3. An ASIC according to claim 1 or 2 wherein one of the communication buses is a data bus.

4. An ASIC according to claim 1, 2 or 3 wherein one of the communication buses is an address bus.

5. An ASIC according to claim 1, 2, 3 or 4 wherein one of the communication buses is a control bus.

6. An ASIC according to any preceding claim wherein at least one of the pins can support bi-directional signals.

7. An ASIC as claimed in claim 1 substantially as herein described, with reference to the accompanying drawings.

8. A method for enabling an ASIC to communicate with an external device, the ASIC comprising a plurality of communication buses, a plurality of pins and means for selecting the internal communication bus to which each pin is connected, the method comprising the steps of: connecting at least some of the pins to the external device and controlling the selecting means to connect a desired internal communication bus to each of the pins connected to the external device.

9. A method according to claim 8 wherein the means for selecting the internal communication bus to which each pin is connected is a multiplexer.

10. A method according to claim 8 or 9 wherein one of the communication buses is a data bus.

11. A method according to claim 8, 9 or 10 wherein one of the communication buses is an address bus.

12. A method according to any of claims 8, 9, 10 or 11 wherein one of the communication buses is a control bus.

13. A method according to any of claims 8 to 12 wherein at least one of the pins can support bi-directional signals.

14. A method as claimed in claim 8 substantially as herein described, with reference to the accompanying drawings.

Application No: GB 0200320.0 **Examiner:** Jim Calvert
Claims searched: 1 **Date of search:** 15 July 2002

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.T):

Int Cl (Ed.7): G06F 1/22, 15/78

Other: Online: EPODOC, WPI, PAJ, XPESP, TDB, INSPEC, EXPLORE

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X	US6119175 A	(GENERAL ELECTRIC) See e.g. column 1, line 15 to column 2, line 15	X:1 Y:1-6, 8-13
Y	WO9745870 A	(MICROCHIP TECH INC) See e.g. column 3, lines 20 to 36	1,3
Y	US5594874 A	(CIRRUS LOGIC) Whole document	1-6, 8-13
Y	US4991085 A	(CHIPS AND TECH INC) See e.g. column 16, line 38 to column 18, line 8	1,2,8,9
Y	US4717912 A	(ADVANCED MICRO DEVICES) Whole document	1,2,8,9

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.